Xilinx Virtex™-E FPGA Development Kit

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Introduction

The Virtex™-E Development Kit provides a complete hardware development environment for FPGA or system designers to accelerate their time to market. With the extensive hardware functions available on the kit, you can begin your FPGA design or applications code development right away, with no need to wait for prototype circuit boards. Unlike other boards that only offer only one or two I/O ports, no memory and little expansion capability, the Virtex-E™ Development Kit offers a majority of functions usually required, as well as the ability to add custom hardware via the PCI bus, a PC card connector, PCI mezzanine connector, and the AvBus™ modular hardware expansion connectors. This kit provides it all, with extensive on board functionality and unmatched expansion capability.

Avnet Design Services has assembled an extensive group of industry leading integrated circuits suppliers, applications code developers, and web partners, as well as IP Cores, device drivers, development tools, and test equipment, to support the Virtex™-E Development Kit. Our partners have chosen the Virtex™-E Development Kit as their system development environment of choice. Visit www.ads.avnet.com/Kit for a current list of our partners, along with their support products and services available to help speed your development cycle.

1.0 Features

The Virtex™-E Development Kit incorporates a variety of hardware resources on a single PCI form factor printed circuit board to create a powerful FPGA and system design development environment. Included on the board are the following hardware resources:

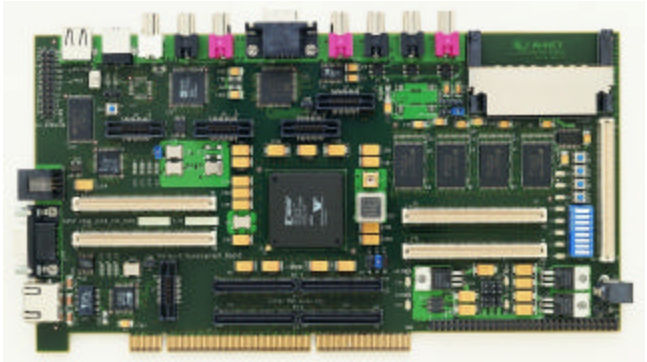
- FPGA / Interfaces
  - Xilinx® Virtex™-E XCV1000E-6FG1156 (660 I/O) (expandable up to the XCV3200E, 804 I/O)
  - Controlled impedance board and I/O connectors
  - 64-Bit/33Mhz, PCI Bus standard interface connector (+3.3 VDC)
  - Supports PCI mezzanine cards (IEEE Std. 1386) (+3.3VDC)
  - AvBus™ daughtercard connectors (5 -140 pin AMP #179031-6)
  - PC card connector
- Memory
  - 64 MByte Micron® SDRAM (Four 16MByte x 16-Bit x 4 banks, to form a 64-Bit bus)
  - 32 MByte Flash (Four 8MByte x 16-Bit, to form a 64-Bit bus); sites for both AMD and Intel (+5.0 VDC and +3.3 VDC) components
- Communication
  - Bi-directional RS232 interface (UART core internal to FPGA)
  - CAN bus interface (CAN core internal to FPGA)
  - 10/100 PHY interface (w/MAC core internal to FPGA)
  - Optional USB 2.0 (and 1.1 compliant) transceiver with one upstream and one downstream connector (USB core internal to FPGA)
- Video / Audio
  - PAL/NTSC/SECAM Video Decoder
  - 80MHz, 256X24 Color Palette, Triple, 6-bit Video Converter, RAM-DAC
  - 192Khz 24 Bit Stereo DAC
- Miscellaneous
  - 8 DIP switches
  - 3 Push-buttons
  - 8 LEDs
- Power
  - On-card power regulation derived from +9.0 VDC
  - +5.0 VDC used to create +3.3 VDC and +1.8 VDC
  - PCI +5.0 VDC option to power card
  - PC card power management controller
- Programming Options
  - Xilinx Serial / Parallel download port
  - FLASH based parallel FPGA loading (SelectMAP)
  - JTAG port

2.0 Ordering Information

The following table lists the development system part number. The internet link is located at: http://www.ads.avnet.com/Kit

Table 1 Virtex™-E Development Kit

Part Number	Hardware
ADS-XLX-VE-DEV	**Virtex™-E Development Kit**



Literature #ADS-001105

3.0 Hardware Design Overview

The following sections provide detailed design information for each of the key sections of the Virtex™-E Development Kit.

3.1 Printed Circuit Board

The printed circuit board (PCB) is 12 layers with six signal layers, a +3.3VDC power plane, a +5.0 VDC power plane incorporating an isolated +1.8 VDC mini-plane, and two ground planes. A controlled impedance of 50 ohms is used within the PCB to ensure consistent signal integrity. The board stack-up is as follows:

1) Component side / Pads / Signal
2) Ground Plane
3) Signal
4) Signal
5) +3.3 VDC
6) Signal
7) Signal
8) +5.0 VDC Plane / +1.8 VDC Plane
9) Signal
10) Signal
11) Ground Plane
12) Pads / Signal

3.2 Virtex™-E FPGA

The Virtex™-E Field-Programmable Gate Array device utilized in this design is the XCV1000E-6FG1156 (660 I/O) in a FG1156 package (fine pitch BGA). This same package accommodates the XCV1600E, XCV2000E, XCV2600E and the XCV3200E, however, a different I/O count is achieved when using the larger components (explained below). Configuration information is provided from two sources; the Xilinx serial/parallel download connector (JTAG), or FLASH configuration memory (SelectMAP).

The Xilinx FPGA is powered at +3.3VDC with the core powered at +1.8 VDC.

3.2.1 Virtex™-E FPGA Installation Options

The following table depicts the logic cell and I/O comparison for each FPGA package option.

Component	Logic Cells/System Gates	I/O Pins
XCV1000E	27,648 / 1,146K – 1,569K	660
XCV1600E	34,992 / 1,628K – 2,189K	724
XCV2000E	43,200 / 1,857K – 2,542K	804
XCV2600E	57,132 / 2,221K – 3,264K	804
XCV3200E	73,008 / 2,608K – 4,074K	804

3.3 Memory

Memory is configured with a 64 bit wide data bus for both the FLASH and SDRAM. A common bus is used to connect the Virtex™-E FPGA, memory, and the memory I/O connectors. Chip selects driven by individual Virtex™-E pins are utilized to enable/tristate the different memory technologies. In addition, all memory control signals (i.e. FLASH and SDRAM) are assigned to the memory connectors to allow a daughter card Evaluation module or Processor module control of the on board memory.

3.3.1 FLASH Memory

The FLASH memory array consists of four 8 Mbyte devices (32 Mbytes total) in a 64-bit configuration. AMD AM29LV641 FLASH memories are installed as the default configuration and are powered by +3.3VDC. Pad locations on the PCB also support Intel FLASH memories and are interchangeable on the board with jumper selections allowing +5.0 VDC and +3.3 VDC components to be installed. The device packages are TSSOP48 (AMD) and TSSOP56 (Intel) and are supported by using a “stacking” layout on the PCB to conserve board area. The current configuration utilizes 90 nanosecond devices, but the Virtex™-E FPGA will support much faster devices. In addition, the FLASH densities may be upgraded to the 128 Mbit components if desired.

3.3.2 SDRAM

The SDRAM array consists of four 16 Mbyte devices (64 Mbytes total) in a 64-bit configuration and housed in TSOP54 packages. The Micron® part number is MT48LC8M16A2TG. These are LVTTL interface devices running at a maximum 66Mhz. Device control, access timing and memory refresh timing are provided by the Virtex™-E FPGA firmware.

3.4 VIDEO / AUDIO

3.4.1 Video RAM-DAC

The ADV478 RAM-DAC incorporates a 256x4 color lookup table with triple 8-bit video D/A converters. The RAM-DAC generates RS343A and RS170 compatible video signals without the need for external buffering.

The control interface is via an eight bit parallel port. The Analog Devices ADV478 is sourced by +5.0VDC volts and is supplied in a PLCC44 package.

3.4.2 Video Decoder

The SAA7114H video decoder is a combination of a two-channel analog preprocessing circuit including source selection, anti-aliasing filter and ADC, an automatic clamp and gain control, a clock generation circuit (CGC), and a digital multi-standard decoder. It also supports a two-dimensional chrominance/luminance separation by an adaptive comb filter and a high performance scaler, including variable horizontal and vertical up and down scaling and a brightness, contrast and saturation control circuit.

The decoder is based on the principle of line-locked clock decoding and is able to decode the color of PAL, SECAM and NTSC signals into ITU 601 compatible color component values. The SAA7114H accepts as analog inputs CVBS or S-video (Y/C) from TV or VCR sources, including weak and distorted signals. An expansion port (X-port) for digital video (bi-directional half duplex, D1 compatible) is also supported to connect to MPEG or a video-phone codec. At the image port (I-port), the SAA7114H supports 8 or 16-bit wide output data with auxiliary reference data for interfacing to VGA controllers.

The decoder device incorporates six video analog inputs with two analog preprocessing channels. The decoder is a +3.3 VDC component in a LQFP100 package.

3.4.3 STEREO AUDIO-DAC

The AD1853 audio DAC supports the 192 kHz sample rate included in the DVD-Audio specification. The AD1853 is fully compatible with sample rates from 32 kHz, up to and including, 192 kHz. It also achieves 120 dB dynamic range and signal-to-noise ratio without muting. The AD1853 features a digital filter with115 dB stop-band-attenuation and a click-less on-chip volume control. An LM833 audio amplifier is used to buffer the speaker outputs.

The Analog Devices ADV1583 is a 24-bit DAC with up to 24 bit word lengths. The control interface with the FPGA is via a serial (SPI) bus. The DAC is a +5.0 VDC component in a SSOP28 package.

3.5 COMMUNICATION

3.5.1 SYNCHRONOUS (RS232) COMMUNICATION INTERFACE

The ADM3222 is a high speed, 2-channel RS232/V.28 interface device operating from a single +3.3 VDC power supply. A single port is utilized to interface with the FPGA. Low power consumption and a shutdown facility are among some of the component highlights. The ADM3222 conforms to the EIA-232E and CCITT V.28 specifications and operates at data rates up to 230 kbps. The AM3222 contains additional enable and shutdown circuitry, and is packaged in an SO20.

3.5.2 CAN INTERFACE

The TJA1050 is the interface between the controller area network (CAN) protocol controller and the physical bus. It supports baud rates from 60 kbaud up to 1 Mbaud. The TJA1050 provides differential transmit capability to the bus and differential receiver capability to the CAN protocol controller and is fully compatible with the “ISO 11898”standard.

A current-limiting circuit on the transmitter output and a thermal safety circuit protects the IC from damage by switching off the transmitter. The component also provides speed select control. The TJA1050 is supplied in a SO8.

3.5.3 USB 2.0 INTERFACE (Optional)

The Philips ISP1501 USB 2.0 peripheral transceiver is a full-function device designed to be used as a USB 2.0 analog front-end for ASICs and FPGAs with built-in USB 'Serial Interface Engine' (SIE) core. Integrating a USB full-speed (FS) transceiver and a high-speed (HS) transceiver,

ISP1501 implements USB 2.0-compliant connectivity for USB 2.0 peripherals. The Philips 2.0 capable Universal Serial Bus transceiver is utilized to implement a single upstream and a single downstream physical USB port capable of 480 Mbps (USB 2.0 expected rates).

Compliant with USB Specification Rev. 2.0, the ISP1501 switches to a USB1.1 legacy interface when it is used to drive full-speed signaling. The 16-bit bidirectional data bus interface to the SIE operates at 30 MHz. The SIE can utilize the 30 MHz clock as a heartbeat clock. In suspend condition, the clock is held at logic high. The ISP1501 uses an external 12 MHz crystal running on the fundamental frequency or an external 12 MHz clock input. The transceiver is a +3.3 VDC component in a PQFP48 package.

3.5 MISCELLANEOUS

Additional interfaces on the board include 8 LEDs, 3 push button switches, and 8 DIP switches.

3.6 CONNECTORS

General I/O, Memory Expansion, PMC, and Auxiliary connector interfaces are provided for user flexibility. The General I/O, Memory Expansion, and Auxiliary connectors are predefined with a common pinout definition to maintain the high-speed signal quality. This pinout standard has been designated as the AvBus connector standard. It is comprised of a 2:1 signal to power/ground ratio and is implemented to ensure signal integrity and controlled impedance continuity. The connectors used are AMP 140 pin, 0.8mm, and realize an effective I/O count of 181 signals.

Various mating height definitions can be implemented to accommodate any mechanical interface constraints with the installation of Development Modules.

3.6.1 MEMORY EXPANSION CONNECTOR INTERFACE

A memory expansion interface connects the memory signals to the Development Module for an option to implement increased memory capabilities, different memory technologies or a host controller. In addition to the standard memory signals, additional spare I/O signals are routed to the connector to allow for arbitration and control. Unknown bus loading from the Development Module must be considered to ensure the local memory bus functionality with all types of Development Modules installed. Two 140 pin connectors are paired to provide this interface.

3.6.2 GENERAL I/O INTERFACE

A general I/O interface allows the user to adapt any desired functionality to the Development Kit backplane for research and development. The FPGA connections to these connectors utilize a high I/O interface, thus allowing the user to select the installation requirements for their Development Module. Two 140 pin connectors are paired to provide this interface.

3.6.3 PCI MEZZANINE CARD (PMC) INTERFACE

Per IEEE Std 1386, 4 connectors are placed in parallel between the FPGA and the PCI standard connector. This interface allows the installation of various industry applications which conform to the PMC (+3.3 VDC) standard, and thus providing the flexibility of implementing multiple functions available commercially. A connector breakout is provided for the IEEE 1386 Analog I/O defined signals.

3.6.4 PC CARD CONNECTOR

A PC Card interface is incorporated in parallel with one of the auxiliary connector interfaces to reduce the pin count required from the FPGA. This allows development with any PC card or Cardbus application (i.e. PCI to PC card development). The standard PC Card interface is provided with a 68-pin connector.

3.6.5 MISCELLANEOUS CONNECTORS

Various support connectors are installed for I/O, power, and programming for the backplane.

I/O connectors includes an Ethernet RJ-45 connector for 10/100 Ethernet, USB down and up stream, video I/O, CAN bus interface, RS232, and a PC card interface.

Power connections include a +9.0 VDC barrel connector for sourcing the power regulators and on board circuitry.

High density Mictor™ connectors are provided which allow accessibility to the signals between the FPGA and the I/O resources on the board. These connectors allow the user to monitor signal flow during the development process of the FPGA cores.

To accommodate programming the FPGA, a Xilinx parallel/serial connector and a JTAG connector are provided.

3.7 PCI BUS

The PCI bus interface is designed as a +3.3 VDC, 64-Bit, 33 MHz interface compatible with PCI LOCAL BUS SPECIFICATION Revision 2.1S. A standard PCI connector is implemented to provide a card connection to a PC kit. In addition, PCI Mezzanine Card (PMC) connectors (per IEEE Std 1386) are provided to support industry PMC applications. The Virtex™-E device is placed as close as possible to the PCI connectors to facilitate clock/signal routing consistent with the requirements imposed by the PCI 2.1S. All PCI functionality is provided by Virtex™-E firmware. The ±12.0 VDC power available from the PCI bus is not used.

If the PCI interface is not required, this board may be plugged into a mating connector and the 87 dedicated Virtex™-E I/O lines may be used for other applications.

3.8 POWER SUPPLY

The power supply for the board provides regulated power from the input source to create +5.0 VDC, +3.3 VDC and +1.8 VDC. An input supply voltage between +7.0 VDC and +9.0 VDC, is provided via a barrel edge connector. On card power regulation is provided by an L4955V5.1, L4955V3.3, and a Texas Instrument TPS75201QPWP +1.8 VDC regulator. The regulators provide two high current outputs (+3.3 VDC and +1.8 VDC) fromthe +5.0 VDC supply. In addition, the board may be powered by the PCI +5.0 VDC when installed in a PC chassis. In this scenario, all power is derived from the PCI backplane, and the barrel connector is not used.

3.9 EVALUATION MODULES

Evaluation modules interface to the Virtex™-E Development Kit backplane, general I/O, memory expansion, and auxiliary interface connectors. Power sources for the module can be switched to allow the card to be powered as a stand alone unit, as well as powered via the backplane when installed.

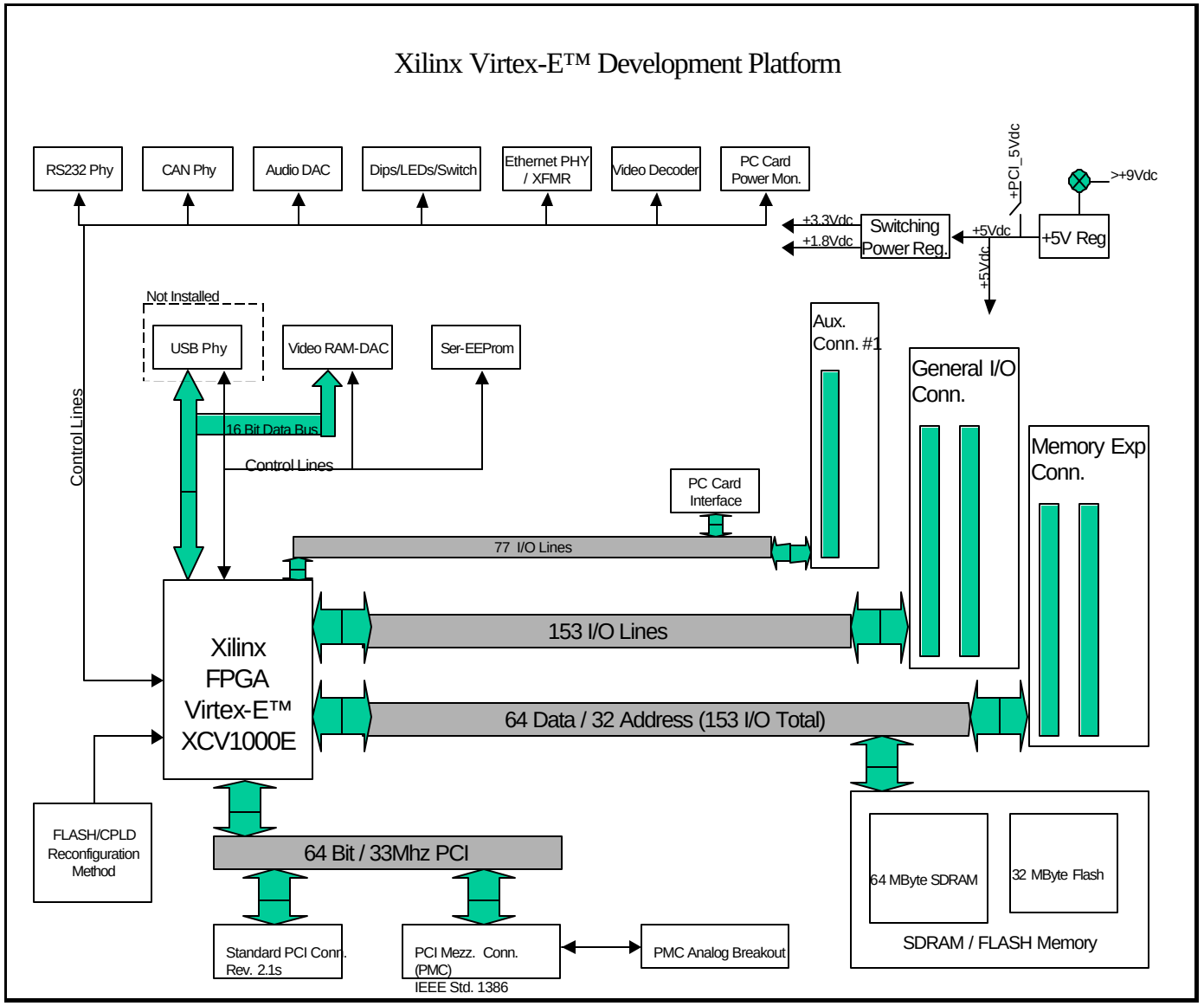
3.10 EVALUATION BOARDS

Evaluation Boards have a primary purpose of being used as a stand alone integration/evaluation tool. However, the Evaluation Board pinout is common to that of the backplane in the event integration between the two kits is desired. Evaluation Boards interface to the Virtex™-E Development Kit backplane via the general I/O interface connector. Power sources for the module are can be switched to allow the card to be powered as a stand alone unit as well powered via the backplane when installed.

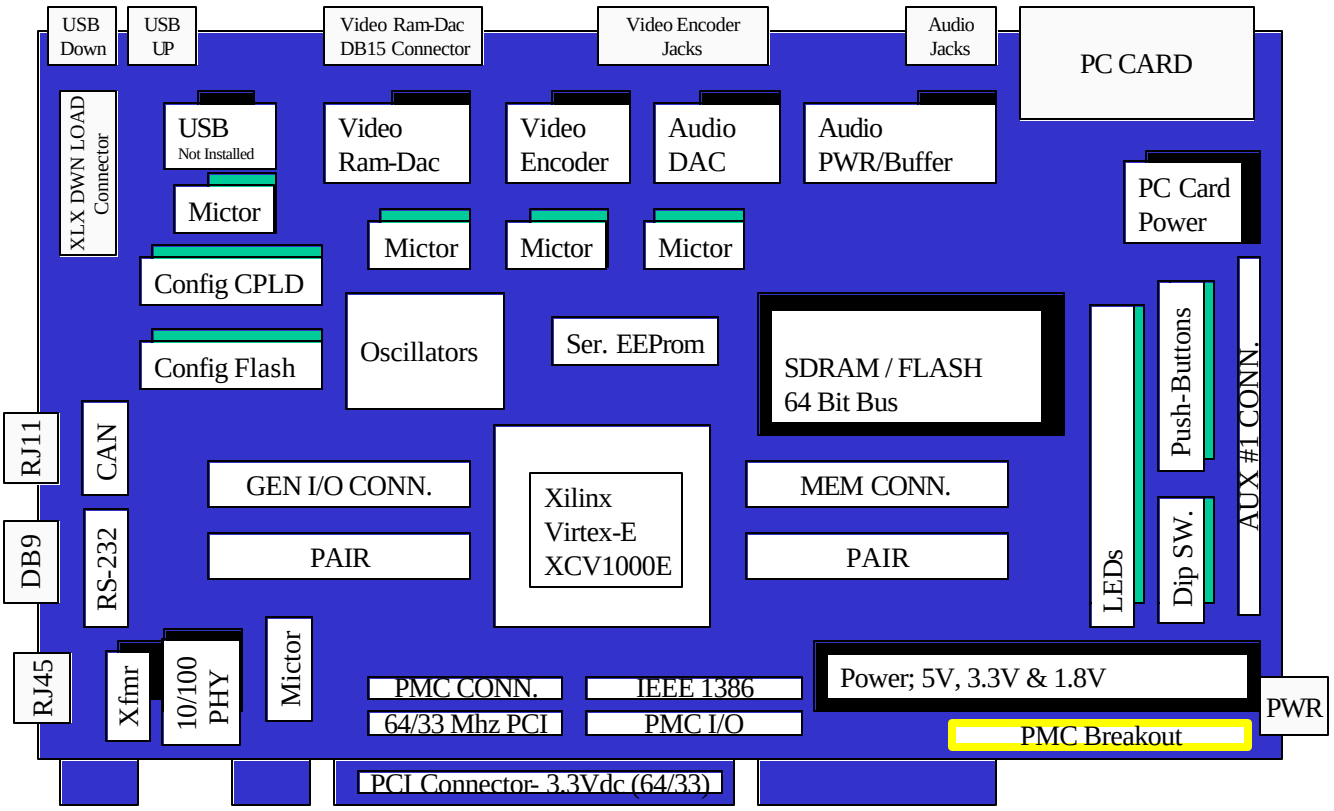
3.11 EXTENDER CARD BOARD

Provisions for an extender card interface may be incorporated on the Development Modules or Boards, which have the same pinout assignment as the backplane connectors. This allows break-out capability of all connector signals for evaluation.

Appendix A: Functional Block Diagram



Appendix B: Board Layout



Optional Components:

U21 - Philips USB Transceiver (LQFP48) – Part Number ISP1501BE
U18 - Burr-Brown DC-DC Converter (SO28) – Part number DCP020515DU

Appendix C: Connector Pinouts

Table 2 JTAG Connector – J20

Signal Name	Download Connector Pin #
D0 / Din	1
D1	2
D2	3
D3	4
D4	5
D5	6
D6	7
D7	8
TDI	9
DONE	10
TCK	11
PROG	12
TMS	13
INIT	14
TDO	15
Dout / BUSY	16
CS	17
R/W	18
GND	19
VCC	20
GND	21
CCLK	22

Table 3 Mode Select – JP1, JP2, JP3

Configuration Mode	Pull-ups	JP3/M2	JP2/M1	JP1/M0
Master-serial	No	OFF / LOW	OFF / LOW	OFF / LOW
Boundary-scan	No	ON / HIGH	OFF / LOW	ON / HIGH
SelectMAP	No	ON / HIGH	ON / HIGH	OFF / LOW
Slave-serial	No	ON / HIGH	ON / HIGH	ON / HIGH
Master-serial	Yes	ON / HIGH	OFF / LOW	OFF / LOW
Boundary-scan	Yes	OFF / LOW	OFF / LOW	ON / HIGH
*SelectMAP	Yes	OFF / LOW	ON / HIGH	OFF / LOW
Slave-serial	Yes	OFF / LOW	ON / HIGH	ON / HIGH

* = Default state

Table 4 Audio Jacks

Signal Name	Connector Reference
Audio High	J2
Audio Low	J3

Table 5 Video Decoder Jacks

Signal Name	Connector Reference
Video-In 1	J12
Video-In 2	J13

Table 6 Ethernet Connector Pinout – P1

Signal Name	RJ45 Connector Def.
Ethernet TX+	1
Ethernet TX-	2
Ethernet RX+	3
N/A	4
N/A	5
Ethernet RX-	6
N/A	7
N/A	8
LED1 Cathode	9
LED1 Anode	10
LED2 Cathode	11
LED2 Anode	12
GND	13
GND	14

Table 7 RS232 Connector Pinout – P2

Signal Name	DB9 Connector Def.
TX out	2
RX in	3
GND	5

Table 8 CAN Connector Pinout – J11

Signal Name	RJ11 Connector Def.
CAN High	3
CAN Low	4
GND	2
GND	5

Table 9 USB Connector Pinout

Signal Name	J8 – Upstream Connector Def.
NC	1
USB -	2
USB +	3
GND	4
SHIELD	5
Signal Name	**J9 – Downstream Connector Def.**
+5Vdc	1
USB -	2
USB +	3
GND	4
SHIELD	5

Table 10 Video Encoder Connector Pinout

Signal Name	RCA Jacks
Video - Green / Y / CVBS	J16
Video – Blue / U / Luma	J17
Video – Red / V / Chroma	J18
Signal Name	**P3 – DB15 Connector Def.**
Video – VSYNC	14
Video – HSYNC	13
Video - Green / Y / CVBS	3
Video – Blue / U / Luma	2
Video – Red / V / Chroma	1

Table 11 PCI Connector and Interface Signals

PCI SIGNAL	PCI PIN #		PCI SIGNAL	PCI PIN #		PCI SIGNAL	PCI PIN #
-12V	B1		GND	B34		C/BE[7]#	A64
TRST#	A1		FRAME#	A34		C/BE[6]#	B65
TCK	B2		IRDY#	B35		C/BE[5]#	A65
+12V	A2		GND	A35		C/BE[4]#	B66
GND	B3		+3.3V	B36		+3.3V	A66
TMS	A3		TRDY# @	A36		GND	B67
TDO	B4		DEVSEL# @	B37		PAR64	A67
TDI	A4		GND	A37		AD[63]	B68
+5V	B5		GND	B38		AD[62]	A68
+5V	B6		STOP# @	A38		AD[61	B69
INTA#	A6		LOCK	B39		GND	A69
INTB#	B7		*3.3V	A39		+3.3V	B70
INTC#	A7		PERR# @	B40		AD[60]	A70
INTD#	B8		SDONE	A40		AD[59]	B71
+5V	A8		+3.3V	B41		AD[58]	A71
PRSNT1#	B9		SBO#	A41		AD[57]	B72
n/c	A9		SERR#	B42		GND	A72
n/c	B10		GND	A42		GND	B73
+3.3V	A10		+3.3V	B43		AD[56]	A73
PRSNT2#	B11		PAR	A43		AD[55]	B74
n/c	A11		C/BE[1]#	B44		AD[54]	A74
n/c	B14		AD[15]	A44		AD[53]	B75
n/c	A14		AD[14]	B45		+3.3V	A75
GND	B15		+3.3V	A45		GND	B76
RST#	A15		GND	B46		AD[52]	A76
CLK	B16		AD[13]	A46		AD[51]	B77
+3.3V	A16		AD[12]	B47		AD[50]	A77
GND	B17		AD[11]	A47		AD[49]	B78
GNT#	A17		AD[10]	B48		GND	A78
REQ#	B18		GND	A48		+3.3V	B79
GND	A18		M66EN $	B49		AD[48]	A79
+3.3V	B19		AD[09]	A49		AD[47]	B80
n/c	A19		GND	B50		AD[46]	A80
AD[31]	B20		GND	A50		AD[45]	B81
AD[30]	A20		GND	B51		GND	A81
AD[29]	B21		GND	A51		GND	B82
+3.3V	A21		AD[08]	B52		AD[44]	A82
GND	B22		C/BE[0]#	A52		AD[43]	B83
AD[28]	A22		AD[07]	B53		AD[42]	A83
AD[27]	B23		+3.3V	A53		AD[41]	B84
AD[26]	A23		+3.3V	B54		+3.3V	A84
AD[25]	B24		AD[06]	A54		GND	B85
GND	A24		AD[05]	B55		AD[40]	A85
+3.3V	B25		AD[04]	A55		AD[39]	B86
AD[24]	A25		AD[03]	B56		AD[38]	A86
C/BE[3]#	B26		GND	A56		AD[37]	B87
IDSEL	A26		GND	B57		GND	A87
AD[23]	B27		AD[02]	A57		+3.3V	B88
+3.3V	A27		AD[01]	B58		AD[36]	A88
GND	B28		AD[00]	A58		AD[35]	B89
AD[22]	A28		+3.3V	B59		AD[34]	A89
AD[21]	B29		+3.3V	A59		AD[33]	B90
AD[20]	A29		ACK64#	B60		GND	A90
AD[19]	B30		REQ64#	A60		GND	B91

PCI SIGNAL	PCI PIN #		PCI SIGNAL	PCI PIN #		PCI SIGNAL	PCI PIN #
GND	A30		+5V	B61		AD[32]	A91
+3.3V	B31		+5V	A61		reserved	B92
AD[18]	A31		+5V	B62		reserved	A92
AD[17]	B32		+5V	A62		reserved	B93
AD[16]	A32		Reserved	B63		GND	A93
C/BE[2]#	B33		GND	A63		GND	B94
+3.3V	A33		GND	B64		Reserved	A94

Table 12 PMC Connectors Pin Assignments

P4 Connector				P5 Connector			
Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
1	TCK	-12V	2	1	+12V	TRST#	2
3	Ground	INTA#	4	3	TMS	TDO	4
5	INTB#	INTC#	6	5	TDI	Ground	6
7	BUSMODE1#	+5V	8	7	Ground	PCI-RSVD*	8
9	INTD#	PCI-RSVD*	10	9	PCI-RSVD*	PCI-RSVD*	10
11	Ground	PCI-RSVD*	12	11	BUSMODE2#	+3.3V	12
13	CLK	Ground	14	13	RST#	BUSMODE3#	14
15	Ground	GNT#	16	15	3.3V	BUSMODE4#	16
17	REQ#	+5V	18	17	PCI-RSVD*	Ground	18
19	V(I/O)	AD[31]	20	19	AD[30]	AD[29]	20
21	AD[28]	AD[27]	22	21	Ground	AD[26]	22
23	AD[25]	Ground	24	23	AD[24]	+3.3V	24
25	Ground	C/BE[3]#	26	25	IDSEL	AD[23]	26
27	AD[22]	AD[21]	28	27	+3.3V	AD[20]	28
29	AD[19]	+5V	30	29	AD[18]	Ground	30
31	V(I/O)	AD[17]	32	31	AD[16]	C/BE[2]#	32
33	FRAME#	Ground	34	33	Ground	PMC-RSVD	34
35	Ground	IRDY#	36	35	TRDY#	+3.3V	36
37	DEVSEL#	+5V	38	37	Ground	STOP#	38
39	Ground	LOCK#	40	39	PERR#	Ground	40
41	SDONE#	SBO#	42	41	+3.3V	SERR#	42
43	PAR	Ground	44	43	C/BE[1]#	Ground	44
45	V(i/O)	AD[15]	46	45	AD[14]	AD[13]	46
47	AD[12]	AD[11]	48	47	Ground	AD[10]	48
49	AD[09]	+5V	50	49	AD[08]	+3.3V	50
51	Ground	C/BE[0]#	52	51	AD[07]	PMC-RSVD	52
53	AD[06]	AD[05}	54	53	+3.3V	PMC-RSVD	54
55	AD[04]	Ground	56	55	PMC-RSVD	Ground	56
57	V(I/O)	AD[03]	58	57	PMC-RSVD	PMC-RSVD	58
59	AD[02]	AD[01]	60	59	Ground	PMC-RSVD	60
61	AD[00]	+5V	62	61	ACK64#	+3.3V	62
63	Ground	REQ64#	64	63	Ground	PMC-RSVD	64

Table 12 Cont. PMC Connectors Pin Assignments

P6 Connector	P7 & P8 Connector

Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
1	PCI-RSVD	Ground	2	1	I/O 1	I/O 2	2
3	Ground	C/BE[7]#	4	3	I/O 3	I/O 4	4
5	C/BE[6]#	C/BE[5]#	6	5	I/O 5	I/O 6	6
7	C/BE[4]#	Ground	8	7	I/O 7	I/O 8	8
9	V(I/O)	PAR64	10	9	I/O 9	I/O 10	10
11	AD[63]	AD[62]	12	11	I/O 11	I/O 12	12
13	AD[61]	Ground	14	13	I/O 13	I/O 14	14
15	Ground	AD[60]	16	15	I/O 15	I/O 16	16
17	AD[59]	AD[58]	18	17	I/O 17	I/O 18	18
19	AD[57]	Ground	20	19	I/O 19	I/O 20	20
21	V (I/O)	AD[56]	22	21	I/O 21	I/O 22	22
23	AD[55]	AD[54]	24	23	I/O 23	I/O 24	24
25	AD[53]	Ground	26	25	I/O 25	I/O 26	26
27	Ground	AD[52]	28	27	I/O 27	I/O 28	28
29	AD[51]	AD[50]	30	29	I/O 29	I/O 30	30
31	AD[49]	Ground	32	31	I/O 31	I/O 32	32
33	Ground	AD[48]	34	33	I/O 33	I/O 34	34
35	AD[47]	AD[46]	36	35	I/O 35	I/O 36	36
37	AD[45]	Ground	38	37	I/O 37	I/O 38	38
39	V (I/O)	AD[44]	40	39	I/O 39	I/O 40	40
41	AD[43]	AD[42]	42	41	I/O 41	I/O 42	42
43	AD[41]	Ground	44	43	I/O 43	I/O 44	44
45	Ground	AD[40]	46	45	I/O 45	I/O 46	46
47	AD[39]	AD[38]	48	47	I/O 47	I/O 48	48
49	AD[37]	Ground	50	49	I/O 49	I/O 50	50
51	Ground	AD[36]	52	51	I/O 51	I/O 52	52
53	AD[35]	AD[34]	54	53	I/O 53	I/O 54	54
55	AD[33]	Ground	56	55	I/O 55	I/O 56	56
57	V (I/O)	AD[32]	58	57	I/O 57	I/O 58	58
59	PCI-RSVD	PCI-RSVD	60	59	I/O 59	I/O 60	60
61	PCI-RSVD	Ground	62	61	I/O 61	I/O 62	62
63	Ground	PCI-RSVD	64	63	I/O 63	I/O 64	64

Table 13 Memory AvBus Connector P9 & P10

Name	P9 Connector Pin #			Name		Name	P10 Connector Pin #			Name
ADDRESS0	71		1	+5V		DATA32	71		1	+5V
GND	72		2	ADDRESS1		GND	72		2	DATA33
ADDRESS3	73		3	ADDRESS2		DATA35	73		3	DATA34
ADDRESS4	74		4	GND		DATA36	74		4	GND
GND	75		5	ADDRESS5		GND	75		5	DATA37
ADDRESS7	76		6	ADDRESS6		DATA39	76		6	DATA38
ADDRESS8	77		7	GND		DATA40	77		7	GND
+3.3V	78		8	ADDRESS9		+3.3V	78		8	DATA41
ADDRESS11	79		9	ADDRESS10		DATA43	79		9	DATA42
ADDRESS12	80		10	GND		DATA44	80		10	GND
GND	81		11	ADDRESS13		GND	81		11	DATA45
ADDRESS15	82		12	ADDRESS14		DATA47	82		12	DATA46
ADDRESS16	83		13	+5V		DATA48	83		13	+5V
GND	84		14	ADDRESS17		GND	84		14	DATA49
ADDRESS19	85		15	ADDRESS18		DATA51	85		15	DATA50
ADDRESS20	86		16	GND		DATA52	86		16	GND
GND	87		17	ADDRESS21		GND	87		17	DATA53
ADDRESS23	88		18	ADDRESS22		DATA55	88		18	DATA54
ADDRESS24	89		19	GND		DATA56	89		19	GND
+3.3V	90		20	ADDRESS25		+3.3V	90		20	DATA57
ADDRESS27	91		21	ADDRESS26		DATA59	91		21	DATA58
ADDRESS28	92		22	GND		DATA60	92		22	GND
GND	93		23	ADDRESS29		GND	93		23	DATA61
ADDRESS31	94		24	ADDRESS30		DATA63	94		24	DATA62
DATA0	95		25	+5V		FLASH_CE2#	95		25	+5V
GND	96		26	DATA1		GND	96		26	FLASH_CE3#
DATA3	97		27	DATA2		SD_BYTE5	97		27	SD_BYTE4
DATA4	98		28	GND		SD_BYTE6	98		28	GND
GND	99		29	DATA5		GND	99		29	SD_BYTE7
DATA7	100		30	DATA6		MEM_IO_7	100		30	MEM_IO_6
DATA8	101		31	GND		MEM_IO_8	101		31	GND
+3.3V	102		32	DATA9		+3.3V	102		32	MEM_IO_9
DATA11	103		33	DATA10		MEM_IO_11	103		33	MEM_IO_10
DATA12	104		34	GND		MEM_IO_12	104		34	GND
GND	105		35	DATA13		GND	105		35	MEM_IO_13
DATA15	106		36	DATA14		MEM_IO_15	106		36	MEM_IO_14
DATA16	107		37	+5V		MEM_IO_16	107		37	+5V
GND	108		38	DATA17		GND	108		38	MEM_IO_17
DATA19	109		39	DATA18		MEM_IO_19	109		39	MEM_IO_18
DATA20	110		40	GND		MEM_IO_20	110		40	GND
GND	111		41	DATA21		GND	111		41	MEM_IO_21
DATA23	112		42	DATA22		MEM_IO_23	112		42	MEM_IO_22
DATA24	113		43	GND		MEM_IO_24	113		43	GND
+3.3V	114		44	DATA25		+3.3V	114		44	MEM_IO_25
DATA27	115		45	DATA26		MEM_IO_27	115		45	MEM_IO_26
DATA28	116		46	GND		MEM_IO_28	116		46	GND
GND	117		47	DATA29		GND	117		47	MEM_IO_29
DATA31	118		48	DATA30		MEM_IO_31	118		48	MEM_IO_30
FLASH_CE0#	119		49	+5V		MEM_IO_32	119		49	+5V
GND	120		50	FLASH_CE1#		GND	120		50	MEM_IO_33
FLASH_WE#	121		51	FLASH_OE#			121		51	
FLASH_RST#	122		52	GND			122		52	GND
GND	123		53	SD_CS#		GND	123		53	
SD_WE#	124		54	SD_CAS#			124		54	
SD_CLK	125		55	GND			125		55	GND
+3.3V	126		56	SD_RAS#		+3.3V	126		56	

Name	P9 Connector Pin #			Name		Name	P10 Connector Pin #			Name
SD_BYTE0	127		57	SD_CLKEN			127		57	
SD_BYTE1	128		58	GND			128		58	GND
GND	129		59	SD_BYTE3		GND	129		59	
MEM_IO_0	130		60	SD_BYTE4			130		60	
MEM_IO_1	131		61	+5V			131		61	+5V
GND	132		62	MEM_IO_2		GND	132		62	
MEM_IO_4	133		63	MEM_IO_3			133		63	
MEM_IO_5	134		64	GND			134		64	GND
GND	135		65	CLK_IN		GND	135		65	
CLK_OUT	136		66	CLK_OUT_FB			136		66	
TMS	137		67	GND			137		67	GND
+3.3V	138		68	TDO		+3.3V	138		68	
TDI	139		69	TCK			139		69	
TRS	140		70	GND			140		70	GND

Table 14 Memory AvBus Connector P11 & P12

Name	P11 Connector Pin #			Name		Name	P12 Connector Pin #			Name
GEN_IO_0	71		1	+5V		GEN_IO_85	71		1	+5V
GND	72		2	GEN_IO_1		GND	72		2	GEN_IO_86
GEN_IO_3	73		3	GEN_IO_2		GEN_IO_88	73		3	GEN_IO_87
GEN_IO_4	74		4	GND		GEN_IO_89	74		4	GND
GND	75		5	GEN_IO_5		GND	75		5	GEN_IO_90
GEN_IO_7	76		6	GEN_IO_6		GEN_IO_92	76		6	GEN_IO_91
GEN_IO_8	77		7	GND		GEN_IO_93	77		7	GND
+3.3V	78		8	GEN_IO_9		+3.3V	78		8	GEN_IO_94
GEN_IO_11	79		9	GEN_IO_10		GEN_IO_96	79		9	GEN_IO_95
GEN_IO_12	80		10	GND		GEN_IO_97	80		10	GND
GND	81		11	GEN_IO_13		GND	81		11	GEN_IO_98
GEN_IO_15	82		12	GEN_IO_14		GEN_IO_100	82		12	GEN_IO_99
GEN_IO_16	83		13	+5V		GEN_IO_101	83		13	+5V
GND	84		14	GEN_IO_17		GND	84		14	GEN_IO_102
GEN_IO_19	85		15	GEN_IO_18		GEN_IO_104	85		15	GEN_IO_103
GEN_IO_20	86		16	GND		GEN_IO_105	86		16	GND
GND	87		17	GEN_IO_21		GND	87		17	GEN_IO_106
GEN_IO_23	88		18	GEN_IO_22		GEN_IO_108	88		18	GEN_IO_107
GEN_IO_24	89		19	GND		GEN_IO_109	89		19	GND
+3.3V	90		20	GEN_IO_25		+3.3V	90		20	GEN_IO_110
GEN_IO_27	91		21	GEN_IO_26		GEN_IO_112	91		21	GEN_IO_111
GEN_IO_28	92		22	GND		GEN_IO_113	92		22	GND
GND	93		23	GEN_IO_29		GND	93		23	GEN_IO_114
GEN_IO_31	94		24	GEN_IO_30		GEN_IO_116	94		24	GEN_IO_115
GEN_IO_32	95		25	+5V		GEN_IO_117	95		25	+5V
GND	96		26	GEN_IO_33		GND	96		26	GEN_IO_118
GEN_IO_35	97		27	GEN_IO_34		GEN_IO_120	97		27	GEN_IO_119
GEN_IO_36	98		28	GND		GEN_IO_121	98		28	GND
GND	99		29	GEN_IO_37		GND	99		29	GEN_IO_122
GEN_IO_39	100		30	GEN_IO_38		GEN_IO_124	100		30	GEN_IO_123
GEN_IO_40	101		31	GND		GEN_IO_125	101		31	GND
+3.3V	102		32	GEN_IO_41		+3.3V	102		32	GEN_IO_126
GEN_IO_43	103		33	GEN_IO_42		GEN_IO_128	103		33	GEN_IO_127
GEN_IO_44	104		34	GND		GEN_IO_129	104		34	GND
GND	105		35	GEN_IO_45		GND	105		35	GEN_IO_130
GEN_IO_47	106		36	GEN_IO_46		GEN_IO_132	106		36	GEN_IO_131
GEN_IO_48	107		37	+5V		GEN_IO_133	107		37	+5V

Name	P11 Connector Pin #		Name		Name	P12 Connector Pin #		Name
GND	108	38	GEN_IO_49		GND	108	38	GEN_IO_134
GEN_IO_51	109	39	GEN_IO_50		GEN_IO_136	109	39	GEN_IO_135
GEN_IO_52	110	40	GND		GEN_IO_137	110	40	GND
GND	111	41	GEN_IO_53		GND	111	41	GEN_IO_138
GEN_IO_55	112	42	GEN_IO_54		GEN_IO_140	112	42	GEN_IO_139
GEN_IO_56	113	43	GND		GEN_IO_141	113	43	GND
+3.3V	114	44	GEN_IO_57		+3.3V	114	44	GEN_IO_142
GEN_IO_59	115	45	GEN_IO_58		GEN_IO_144	115	45	GEN_IO_143
GEN_IO_60	116	46	GND		GEN_IO_145	116	46	GND
GND	117	47	GEN_IO_61		GND	117	47	GEN_IO_146
GEN_IO_63	118	48	GEN_IO_62		GEN_IO_148	118	48	GEN_IO_147
GEN_IO_64	119	49	+5V		GEN_IO_149	119	49	+5V
GND	120	50	GEN_IO_65		GND	120	50	GEN_IO_150
GEN_IO_67	121	51	GEN_IO_66			121	51	
GEN_IO_68	122	52	GND			122	52	GND
GND	123	53	GEN_IO_69		GND	123	53	
GEN_IO_71	124	54	GEN_IO_70			124	54	
GEN_IO_72	125	55	GND			125	55	GND
+3.3V	126	56	GEN_IO_73		+3.3V	126	56	
GEN_IO_75	127	57	GEN_IO_74			127	57	
GEN_IO_76	128	58	GND			128	58	GND
GND	129	59	GEN_IO_77		GND	129	59	
GEN_IO_79	130	60	GEN_IO_78			130	60	
GEN_IO_80	131	61	+5V			131	61	+5V
GND	132	62	GEN_IO_81		GND	132	62	
GEN_IO_83	133	63	GEN_IO_82			133	63	
GEN_IO_84	134	64	GND			134	64	GND
GND	135	65	GEN_IO_CLK_OUT		GND	135	65	
GEN_IO_CLKIN	136	66	GEN_IO_CLK_FB			136	66	
TMS	137	67	GND			137	67	GND
+3.3V	138	68	TDIO_3		+3.3V	138	68	
TDIO_2	139	69	TCK			139	69	
TRST#	140	70	GND			140	70	GND

Table 15 AvBus Connector P2

Name	Connector PIN #			Name
AUX_IO_0	71		1	+5V
GND	72		2	AUX_IO_1
AUX_IO_3	73		3	AUX_IO_2
AUX_IO_4	74		4	GND
GND	75		5	AUX_IO_5
AUX_IO_7	76		6	AUX_IO_6
AUX_IO_8	77		7	GND
+3.3V	78		8	AUX_IO_9
AUX_IO_11	79		9	AUX_IO_10
AUX_IO_12	80		10	GND
GND	81		11	AUX_IO_13
AUX_IO_15	82		12	AUX_IO_14
AUX_IO_16	83		13	+5V
GND	84		14	AUX_IO_17
AUX_IO_19	85		15	AUX_IO_18
AUX_IO_20	86		16	GND
GND	87		17	AUX_IO_21
AUX_IO_23	88		18	AUX_IO_22
AUX_IO_24	89		19	GND
+3.3V	90		20	AUX_IO_25
AUX_IO_27	91		21	AUX_IO_26
AUX_IO_28	92		22	GND
GND	93		23	AUX_IO_29
AUX_IO_31	94		24	AUX_IO_30
AUX_IO_32	95		25	+5V
GND	96		26	AUX_IO_33
AUX_IO_35	97		27	AUX_IO_34
AUX_IO_36	98		28	GND
GND	99		29	AUX_IO_37
AUX_IO_39	100		30	AUX_IO_38
AUX_IO_40	101		31	GND
+3.3V	102		32	AUX_IO_41
AUX_IO_43	103		33	AUX_IO_42
AUX_IO_44	104		34	GND
GND	105		35	AUX_IO_45
AUX_IO_47	106		36	AUX_IO_46
AUX_IO_48	107		37	+5V
GND	108		38	AUX_IO_49
AUX_IO_51	109		39	AUX_IO_50
AUX_IO_52	110		40	GND
GND	111		41	AUX_IO_53
AUX_IO_55	112		42	AUX_IO_54
AUX_IO_56	113		43	GND
+3.3V	114		44	AUX_IO_57
AUX_IO_59	115		45	AUX_IO_58
AUX_IO_60	116		46	GND
GND	117		47	AUX_IO_61
AUX_IO_63	118		48	AUX_IO_62
AUX_IO_64	119		49	+5V
GND	120		50	AUX_IO_65
AUX_IO_67	121		51	AUX_IO_66
AUX_IO_68	122		52	GND

Name	Connector PIN #			Name
GND	123		53	AUX_IO_69
AUX_IO_71	124		54	AUX_IO_70
AUX_IO_72	125		55	GND
+3.3V	126		56	AUX_IO_73
	127		57	AUX_IO_74
	128		58	GND
GND	129		59	
AUX_IO_75	130		60	
AUX_IO_76	131		61	+5V
GND	132		62	AUX_IO_77
AUX_IO_79	133		63	AUX_IO_78
AUX_IO_80	134		64	GND
GND	135		65	AUX_IO_CLKOUT
AUX_IO_CLKIN	136		66	AUX_IO_CLK_FB
TMS	137		67	GND
+3.3V	138		68	TDO
TDI	139		69	TCK
TRST	140		70	GND

Table 16 Mictor Connector – J14

Pin	Name	Name	Pin
1			2
3			4
5	VID_D_CLK	VID_D_XPD7	6
7	VID_D_HPD0	VID_D_XPD6	8
9	VID_D_HPD1	VID_D_XPD5	10
11	VID_D_HPD2	VID_D_XPD4	12
13	VID_D_HPD3	VID_D_XPD3	14
15	VID_D_HPD4	VID_D_XPD2	16
17	VID_D_HPD5	VID_D_XPD1	18
19	VID_D_HPD6	VID_D_XPD0	20
21	VID_D_HPD7	VID_D_CE_RESET#	22
23	VID_D_IPD0	VID_D_CE	24
25	VID_D_IPD1	VID_D_ITRDY	26
27	VID_D_IPD2	VID_D_ITRI	28
29	VID_D_IPD3	VID_D_IDQ	30
31	VID_D_IPD4	VID_D_IPGV	32
33	VID_D_IPD5	VID_D_IPGH	34
35	VID_D_IPD6	VID_D_IPG0	36
37	VID_D_IPD7	VID_D_IPG1	38

Table 17 Mictor Connector – J15

Pin	Name	Name	Pin
1			2
3			4
5	AUD_VID_24.576MHZ	VID_D_ICLK	6
7			8
9		AUDIO_CLATCH	10
11	VID_D_XTRI	AUDIO_CCLK	12
13	VID_D_XCLK	AUDIO_MUTE	14
15	VID_D_XDQ	AUDIO_DEEMP	16
17	VID_D_XRDY	AUDIO_IDPM1	18
19	VID_D_XRV	AUDIO_IDPM0	20

Pin	Name	Name	Pin
21	VID_D_XRH	AUDIO_CDATA	22
23	VID_D_RTS1	AUDIO_BLCK	24
25	VID_D_RTS0	AUDIO_L/RCLK	26
27	VID_D_RTC0	AUDIO_SDATA	28
29	VID_D_LLC2	AUDIO_INT4X	30
31	VID_D_LLC	AUDIO_INT4X	32
33	I2C_SCLK	AUDIO_RESET#	34
35	I2C-SDA	AUDIO_ZEROL	36
37		AUDIO_ZEROR	38

Table 18 Mictor Connector – J7

Pin	Name	Name	Pin
1			2
3			4
5		ENET_25MHZ_XI	6
7	ENET_TXD3		8
9	ENET_TXD2		10
11	ENET_TXD1		12
13	ENET_TXD0	ENET_RX_COL	14
15		ENET_RX_CRS	16
17	ENET_RXD3	ENET_RX_ER	18
19	ENET_RXD2	ENET_RX_DV	20
21	ENET_RXD1	ENET_RX_CLK	22
23	ENET_RXD0	ENET_TX_ER	24
25	ENET_LED/CFG3	ENET_TX_EN	26
27	ENET_LED/CFG2	ENET_TX_CLK	28
29	ENET_LED/CFG1	ENET_MDDIS	30
31	ENET_PAUSE	ENET_MDINT#	32
33	ENET_SLEEP	ENET_MDC	34
35	ENET_PWRDWN	ENET_MDIO	36
37		ENET_RESET#	38

Table 19 Mictor Connector – J10

Pin	Name	Name	Pin
1			2
3			4
5	USB_CLKOUT	VID_E_CLKOUT	6
7		IO_D15	8
9		IO_D14	10
11	USB_DDIR	IO_D13	12
13	USB_RX_VLD	IO_D12	14
15	USB_RX_IN	IO_D11	16
17	USB_RX_BS_ERR	IO_D10	18
19	USB_RX_LBYTE	IO_D9	20
21	USB_TX_RDY	IO_D8	22
23	USB_NRZ_EN_VO	IO_D7	24
25	USB_TX_LAST_BYTE	IO_D6	26
27	USB_BSENN_FSEO	IO_D5	28
29	USB_OE	IO_D4	30
31	USB_SUSPEND	IO_D3	32
33	USB_RESET#	IO_D2	34
35	USB_MODE1	IO_D1	36
37	USB_MODE0	IO_D0	38

Table 20 Mictor Connector – J24

Pin	Name	Name	Pin
1			2
3			4
5	CFG_USB_12MHZ	VID_DAC_CLK	6
7		VID_DAC_BLNK#	8
9		VID_DAC_RD#	10
11		VID_DAC_SYNC#	12
13		VID_DAC_OL3	14
15		VID_DAC_OL2	16
17		VID_DAC_OL1	18
19		VID_DAC_OL0	20
21			22
23			24
25		VID_DAC_WR#	26
27			28
29			30
31		VID_DAC_RS2	32
33		VID_DAC_RS1	34
35	VID_DAC_HSYNC	VID_DAC_RS0	36
37	VID_DAC_VSYNC	SER_EEPROM_DATA	38